Proceedings of the IEEE

January 2019 / VOL. 107 / NO. 1

CONTENTS

SPECIAL ISSUE

NONSILICON, NON-VON NEUMANN COMPUTING—PART I

Edited by S. Basu, R. E. Bryant, G. De Micheli, T. Theis, and L. Whitman

Novel Materials and Devices

19 The N3XT Approach to Energy-Efficient Abundant-Data Computing
By M. M. Sabry Aly, T. F. Wu, A. Bartolo, Y. H. Malviya, W. Hwang, G. Hills, I. Markov, M. Wootters, M. M. Shulaker, H.-S. P. Wong, and S. Mitra

|INVITED PAPER| This paper enables energy-efficient computing for transformative abundant-data applications through heterogeneous integration of energy-efficient logic devices immersed in dense nonvolatile memory, with fine-grained connectivity in a monolithic 3-D architecture.

49 Negative Capacitance Transistors
By J. C. Wong and S. Salahuddin

|INVITED PAPER| This paper provides an overview of a groundbreaking theoretical and experimental work on this promising new type of field-effect transistor.

63 DNA Data Storage and Hybrid Molecular–Electronic Computing
By D. Carmean, L. Ceze, G. Seelig, K. Stewart, K. Strauss, and M. Willsey

|INVITED PAPER| This paper attempts to address the problem of long-term storage and retrieval of large volumes of data based on emerging DNA technology.

Physics-Based Non-von Neumann Paradigm

73 Computing With Networks of Oscillatory Dynamical Systems
By A. Raychowdhury A. Parihar, G. H. Smith, V. Narayanan, G. Csaba, M. Jerry, W. Porod, and S. Datta

|INVITED PAPER| This paper discusses a computing architecture inspired by physics, via the radically different approach of using arrays of oscillators.

90 Shannon-Inspired Statistical Computing for the Nanoscale Era
By N. R. Shanbhag, N. Verma, Y. Kim, A. D. Patil, and L. R. Varshney

|INVITED PAPER| This paper considers a principled information-theoretic approach to the design of non-von Neumann architectures via statistical computing which leverages information-based metrics.

Neuromorphic Paradigm

108 The Next Generation of Deep Learning Hardware: Analog Computing
By W. Haensch, T. Gokmen, and R. Puri

|INVITED PAPER| This paper explores the current state of neuromorphic deep learning architectures in silicon CMOS technology.

123 Efficient Biosignal Processing Using Hyperdimensional Computing: Network Templates for Combined Learning and Classification of ExG Signals
By A. Rahimi, P. Kanerva, L. Benini, and J. M. Rabaey

|INVITED PAPER| This paper takes an unconventional approach to learning machines based on little explored but much promising notion of hyperdimensional computing.

[*Continued on page 2* ➤]

DEPARTMENTS

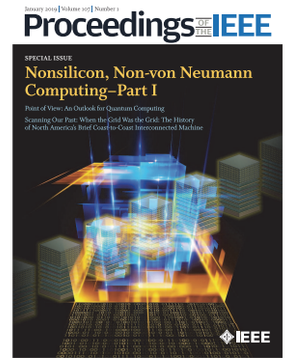
3 POINT OF VIEW
The Best Job in the IEEE
By H. J. Trussell

5 POINT OF VIEW
An Outlook for Quantum Computing
By D. Maslov, Y. Nam, and J. Kim

11 SCANNING THE ISSUE
Nonsilicon, Non-von Neumann Computing—Part I
By S. Basu, R. E. Bryant, G. De Micheli, T. Theis, and L. Whitman

232 SCANNING OUR PAST
When the Grid Was *the Grid*: The History of North America's Brief Coast-to-Coast Interconnected Machine
By J. Cohn

244 FUTURE SPECIAL ISSUE/SPECIAL SECTIONS



On the Cover:
The cover image is an abstract conception inspired by new forms of computing in a nonsilicon environment for coming generations of transformative applications, such as artificial intelligence on massive data. The building blocks shown on the cover are those of N3XT 3D NanoSystems (N3XT=Nano-Engineered Computing Systems Technology). Photo credit: Prof. Subhasish Mitra (Stanford) and Prof. Max Shulaker (MIT).

CONTENTS

CONTINUED FROM PAGE 1

Special Issue: Nonsilicon, Non-von Neumann Computing—Part I

144 Braindrop: A Mixed-Signal Neuromorphic Architecture With a Dynamical Systems-Based Programming Model
By A. Neckar, S. Fok, B. V. Benjamin, T. C. Stewart, N. N. Oza, A. R. Voelker, C. Eliasmith, R. Manohar, and K. Boahen

|INVITED PAPER| This paper provides an overview of a current approach for the construction of a programmable computing machine inspired by the human brain.

CMOS and High-Performance Computing

165 Logic Synthesis for Established and Emerging Computing
By E. Testa, M. Soeken, L. G. Amarù, and G. De Micheli

|INVITED PAPER| This paper provides a state-of-the-art view on the status of logic design flows in conventional silicon CMOS as well as using several of the emerging technologies.

185 Customizable Computing—From Single Chip to Datacenters
By J. Cong, Z. Fang, M. Huang, P. Wei, D. Wu, and C. H. Yu

|INVITED PAPER| This paper deals with the important issue of specialization in designing computing hardware that can potentially provide at least a near-term strategy to combat Moore's law slowdown.

204 Architecture and Advanced Electronics Pathways Toward Highly Adaptive Energy-Efficient Computing
By G. P. Fettweis, M. Dörpinghaus, J. Castrillon, A. Kumar, C. Baier, K. Bock, F. Ellinger, A. Fery, F. H. P. Fitzek, H. Härtig, K. Jamshidi, T. Kissinger, W. Lehner, M. Mertig, W. E. Nagel, G. T. Nguyen, D. Plettemeier, M. Schröter, and T. Strufe

|INVITED PAPER| This paper describes a leading European effort on applications of basic technologies to energy-efficient servers and high-performance computing of the future, that has been ongoing for more than a decade.